

by the value of the external capacitor or output voltage. For example, if the external capacitor is altered, the current required for the switching regulator to enter or exit the low power mode will be changed. Furthermore, in conventional
5 switching regulators, if the voltage of the input driver changes, the point that the switching regulator enters or exits low power mode will change.

Amendments to the Claims:

10

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

15

- 1 1. (currently amended) A switching regulator, comprising:
2 a driver coupled to receive a first high side
3 control signal [reference voltage];
4 an input switching device having a source node, a
5 drain node, and a control node, the control node coupled
6 to an output of the driver, the drain node coupled to
7 receive an input voltage;
8 a diode coupled between the source node of the input
9 switching device and ground;
10 an inductor having a first end coupled to the source
11 node of the input switching device;
12 a first output switching device having a drain node
13 coupled to the second end of the inductor, the first
14 output switching device having a control node coupled to
15 a second high side control signal [output];
16 a second output switching device having a drain node
17 coupled to the second end of the inductor, the [first]

18 second output switching device having a control node
19 coupled to a low side control signal [output], the second
20 output switching device having a source node coupled to
21 ground;
22 an output load coupled [to] between the source nodes
23 of the first and second output switching devices;
24 an output capacitor coupled between the source nodes
25 of the first and second output switching devices to
26 provide an output voltage; and
27 a low power control circuit coupled across the
28 inductor, wherein the low power control circuit monitors
29 the current [across] delivered to the output load and
30 automatically initiates the low power mode of the
31 switching regulator independent of the value of the
32 output voltage, the output capacitor, the inductor [load]
33 and the input voltage.

1 2. (currently amended) A switching regulator as recited
2 in claim 1, wherein the low power control circuit comprises:
3 a low power switching device having a control node
4 coupled to receive the high side control signal [output]
5 and a drain node coupled to the second end of the
6 inductor;
7 an amplifier coupled to the source node of the low
8 power switching device and the first output switching
9 device;
10 a first current mirror coupled to the amplifier to
11 mirror [the difference between] the output current
12 delivered to [through] the output load [and the current
13 supplied at the second end of the inductor] through the
14 low power switching device;
15 a second current mirror coupled to the first current
16 mirror;

17 a current source coupled between [to] the second
18 current mirror and ground;

19 a capacitor coupled across the current source;

20 a comparator coupled to the second current mirror
21 and coupled to receive a predetermined voltage source to
22 compare the voltage across the capacitor with the
23 predetermined voltage source;

24 a first AND gate coupled to the comparator and to
25 receive the low power mode signal;

26 an inverter coupled to receive the low power mode
27 signal to generate an inverted low power mode signal;

28 a second AND gate coupled to the comparator and to
29 receive the inverted low power mode signal and the
30 inductive switch signal;

31 a first counter, having an input and an output, the
32 input coupled to the first AND gate to provide a low
33 power entry signal at the output, the output coupled to
34 the second AND gate; and

35 a second counter, having an input and an output, the
36 input coupled to the second AND gate to provide a low
37 power exit signal at the output, the output coupled to
38 the first AND gate.

1 3. (original) The switching regulator as recited in
2 claim 1, wherein the first input switching device is a
3 transistor.

1 4. (original) The switching regulator as recited in
2 claim 1, wherein the second input switching device is a
3 transistor.

1 5. (original) The switching regulator as recited in
2 claim 1, wherein the first output switching device is a
3 transistor.

1 6. (original) The switching regulator as recited in
2 claim 1, wherein the second output switching device is a
3 transistor.

1 7. (original) The switching regulator as recited in
2 claim 1, wherein the first input switching device is a
3 metal-oxide-semiconductor field-effect transistor (Mos
4 FET).

1 8. (original) The switching regulator as recited in
2 claim 1, wherein the second input switching device is a Mos
3 FET transistor.

1 9. (original) The switching regulator as recited in
2 claim 1, wherein the first output switching device is a
3 Mos FET transistor.

1 10. (original) The switching regulator as recited in
2 claim 1, wherein the second output switching device is a
3 Mos FET transistor.

1 11. (currently amended) The switching regulator as
2 recited in claim 1, wherein the output load [comprises:
3 a capacitor; and] is
4 a resistor [coupled in parallel with the capacitor].

1 12. (original) The switching regulator as recited in
2 claim 2, wherein the low power switching device is a
3 transistor.

1 13. (original) The switching regulator as recited in
2 claim 2, wherein the low power switching device is a
3 sense FET transistor.

1 14. (currently amended) The switching regulator as
2 recited in claim 2, wherein the first current mirror,
3 comprises:

4 a first transistor, having a drain node coupled to
5 the source node of the low power switching device; and

6 a second transistor coupled to the first transistor,
7 the control node of the first and second transistors
8 coupled to the amplifier, the source node of the second
9 transistor coupled to the source node of the first
10 transistor.

1 1[3]5. (currently amended) The switching regulator as
2 recited in claim 2, wherein the second current mirror,
3 comprises:

4 a first transistor, having a drain node, a source
5 node, and a control node, the drain node coupled to the
6 control node and the drain node coupled to the first
7 current mirror; and

8 a second transistor having a drain node, a control
9 node and a source node, the control node coupled to the
10 control node of the first transistor, the source node
11 coupled to the source node of the first transistor, the
12 drain node coupled to the capacitor.